REMARKS / ARGUMENTS

Claims 21-52 remain pending in this application. No claims have been canceled or added.

Title

Applicants have amended the title. The title suggested by the Examiner has been adopted.

Interview

Applicants wish to thank the Examiner and the Examiner's Supervisor for conducting an interview with the undersigned and Applicant's representative on October 23, 2007. The following arguments were presented during the interview.

35 U.S.C. § 103

Claims 21-53 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hubis et al (U.S. Patent No. 6,343,324) in view of Kuchta et al (U.S. Patent No. 6,014,319). These rejections are traversed as follows.

The independent claims, except for claim 21, have been amended as discussed during the interview. Namely, these claims have been amended to recite that the processor adapter determines a location to which data should be written to or read from. While such an amendment was discussed during the interview, upon

further consideration, Applicants conclude that no amendment should be necessary. Applicants believe that the Examiner has a better understanding of the invention so as to be able to see the clear distinction between the present invention and the cited references. Claim 21 has been amended for formal matters.

According to the storage system of the present invention, the processor adaptors are separated from the interface adaptors and provide more flexibility to the storage system by providing the capability to add or remove processor adaptors independently of the interface adaptors. Such flexibility was not present in the prior art.

A good description of the prior art structure of interface units is provided by a reference to Ninomiya et al (U.S. Patent No. 6,012,119) cited in a continuation application of this application and having Serial No. 11/031,556. The Ninomiya reference and others cited in the prosecution of the continuation application are submitted in an accompanying IDS. In Fig. 2 of Ninomiya et al, details of the host adapter 1 and disk adapter 2 are illustrated. The host adapter 1 includes a microprocessor (MP) 10, which receives a data transmission request from a host computer and controls data transmission within host adapter 1 (see column 5, lines 7-10). The disk adapter 2 is under the data transmission control of an MP peripheral (including MP 10, etc.) having the same structure as host adapter 1 (see column 5, lines 33-38). Clearly, Ninomiya et al disclose a structure in which the processors (MPs) are inside the host adapter 1 and disk adapter 2. Therefore, the

number of processor units cannot be changed independently of the number of adapters.

None of the cited references disclose a storage system having a plurality of processor adaptors, first interface adaptors, and second interface adaptors as claimed. Hubis et al disclose a processor 81 that determines access permission and performs scheduling. Therefore, processor 81 of Hubis et al cannot be considered to be one of the processor adaptors of the pending claims.

The pending claims clearly recite the interaction between the interface adapters and the processor adapters. For example, claim 21 recites "a plurality of first interface adapters each coupled to said at least one host computer and receiving a write request and data sent from said at least one host computer and sending a first control information related to said write request to at least one of said processor adapters and sending data received at each of said first interface adapters based on a second control information sent from said at least one processor adapter". This portion of claim 21 refers to the control information sent from the interface adapters to one processor adapter and *vice versa*.

On the other hand, this type of communication does not occur between the Fibre Channel I/O Processors 184 (such as an Intelligent SCSI Processor chip) of Hubis and processor 180 of controller 106 which executes program product 301 corresponding to procedure 300, which in turn determines access permission and performs scheduling.

The deficiencies in Hubis et al are not overcome by resort to Kuchta et al. Kuchta et al merely disclose duplicate card cages 203 and 204 housing electronic circuit cards and other modules which perform the basic logical functions of a system 100 (see column 5, lines 33-36). Each cage includes a processor card 241 which forms the central processing unit (CPU). As shown in Fig. 2B, I/O modules 209-212 are provided to communicate with host computers or storage devices (see column 5, lines 47-58). Modules 205 and 206 are intended as optional performance enhancement modules such as a cache or other logic (see column 5, lines 63-66). Modules 207 and 208 are intended as additional non-volatile random access memory (NV RAM)(see column 5, line 66 to column 6, line 2). None of these modules correspond to the claimed processor adaptor of the present invention, the number of which can be increased or decreased independently of the interface adaptors.

As mentioned in the specification, by providing an independent processor adaptor (such as processor unit 81 in Fig. 1), it is possible to increase/decrease the number of microprocessors independently from the increase/decrease of the number of interfaces connected with server 3 or hard drives 2 (see Specification, page 28, lines 1-5). This makes it possible to provide a storage system having a flexible configuration that can flexibly support user demands, such as the number of connected servers 3 and hard drives 2, as well as system performance (see Specification, page 28, lines 1-8).

As such, it is submitted that the pending claims patentably define the present invention over the cited references. The Examiner is hereby invited to contact the undersigned by telephone with any questions.

Conclusion

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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